What is claimed is:

1. A branch history information write control device in an instruction execution processing apparatus comprising:

a memory unit storing an instruction string;

a branch prediction unit performing a branch prediction of a branch instruction; and

a control unit controlling in such a way that writing of branch history information in the branch prediction unit and control over the memory unit may not occur simultaneously.

2. The device according to claim 1, wherein said control unit writes the branch history information in said branch prediction unit in a timing such that said memory unit cannot accept an instruction fetch request.

3. The device according to claim 1, wherein said control unit writes the branch history information in said branch prediction unit in a timing for making an instruction pre-fetch request.

4. The device according to claim 1, wherein when

writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in said branch prediction unit after several clock cycles (several states).

5. The device according to claim 1, wherein when writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch request is executed.

6. The device according to claim 1, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

said control unit writes the branch history information of the branch instruction in said branch prediction unit several clock cycles (several states)

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after there is a write request of a branch instruction if the temporary instruction buffer unit is empty and there is no instruction fetch request.

7. The device according to claim 1, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

said control unit does not promptly write a branch history of a branch instruction to be requested to be written in said branch prediction unit, waits for a next instruction fetch request and writes the branch history information of the branch instruction several clock cycles (several states) after the instruction fetch request is executed if the temporary instruction buffer unit is empty and there is not even one instruction fetch request.

8. The device according to any one of claims 4 through 7, wherein said control unit uses a counter to count the several clock cycles (several states).

9. The device according to claim 1, wherein when writing the branch history information of the branch

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instruction which has failed in the branch prediction, said control unit writes the branch history information after an instruction decoding unit or said temporary instruction buffer unit in the instruction execution processing apparatus receives a fetch instruction string corresponding to a re-instruction fetch requested by the branch instruction.

10. The device according to claim 1, further comprising:

a write reservation station unit temporarily storing the branch history information to be written.

11. The device according to claim 10, wherein said control unit registers in the reservation station unit only the branch history information concerning a branch instruction which must be written in said branch prediction unit.

12. The device according to claim 11, wherein the branch history information is about at least one of a new entry registration, an entry content change or an entry erasure.

13. The device according to claim 10, wherein if said

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write reservation station unit is full and there is a request for registering in the write reservation station unit, said control unit writes in said branch prediction unit at least one group of branch history information, writing of which in the write reservation station unit is held and the branch history information of which has been requested to be registered.

14. The device according to claim 10, wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and said write reservation station unit stores a plurality of valid information, writing of which is held, said control unit simultaneously writes the plurality of information in a timing such that writing in said branch prediction unit is possible.

15. The device according to claim 1 or 10, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, etc., which exits before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed, and even if the

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branch instruction cannot be completed, said control unit writes the branch history information of the branch instruction in said branch prediction unit or registers the information in the write reservation station unit.

16. The device according to claim 15, wherein said control unit provides a flag indicating that the branch history information is written or registered in the write reservation station unit for each corresponding branch instruction being processed.

17. A branch history information write control device in an instruction execution processing apparatus provided with a branch prediction unit performing a branch prediction of a branch instruction, comprising:

a return address stack unit; and

a control unit writing branch history information in the branch prediction unit, but controlling in such a way not to operate the return address stack if the branch instruction corresponds to a sub-routine call or return and the branch instruction is not executed although a write request of the branch history information of the branch instruction is issued to the branch prediction unit.

18. The device according to claim 10, wherein said control unit writes the branch history information, writing of which in the write reservation station unit is held when an execution of an instruction is completed.

19. The device according to claim 10, wherein said control unit writes branch history information of a corresponding entry in said branch prediction unit or said write reservation station unit when an execution of an instruction is completed.

20. The device according to claim 10, wherein if the instruction execution processing apparatus is provided with a unit controlling an execution completion of an instruction in its instruction control unit,

said control unit stores an ID assigned for each instruction, which is stored in the execution completion management unit, in an entry of the write reservation station unit.

21. The device according to claim 10, wherein if it is confirmed that a branch instruction corresponding to a valid entry of the write reservation station unit is neither executed nor completed due to an occurrence

of interruption, etc., the entry corresponding to the write reservation station unit is nullified.

22. The device according to claim 1, further comprising:

a bypass unit making branch history information, writing of which in said branch prediction unit is held, a research target of a branch prediction.

23. The device according to claim 10, further comprising:

a bypass unit making branch history information of a branch instruction which is being executed in its branch execution unit including the write reservation station unit, a research target of a branch prediction.

24. The device according to claim 23, wherein said bypass unit makes the branch history information a search target of a branch prediction when a conditional code for the branch instruction is confirmed if it is confirmed that the branch instruction is not branched and when a branch destination address is confirmed if it is confirmed that the branch instruction is branched.

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25. The device according to claim 1, wherein a dual-port RAM in which writing and reading can be simultaneously executed independently is used for said branch prediction unit to hold an entry.

26. An instruction control method in an apparatus provided with both a memory storing an instruction string, etc., and a branch prediction unit performing a branch prediction of a branch instruction, comprising:

controlling in such a way that writing of branch history information in said branch prediction unit and control over the memory do not occur simultaneously.

27. The method according to claim 26, wherein the branch history information is written in said branch prediction unit in a timing such that said memory cannot accept an instruction fetch request.

28. The method according to claim 26, wherein the branch history information is written in said branch prediction unit in a timing of requesting a pre-fetch of an instruction.

29. The method according to claim 26, wherein if the

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branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written in said branch prediction unit after several clock cycles (several states).

30. The method according to claim 26, wherein if the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch request is executed.

31. The method according to claim 26, further comprising:

temporary instruction buffer step temporarily storing an instruction string, etc., outputted by said memory,

wherein if there is no instruction string to be stored in the temporary instruction buffer step and there is no instruction fetch request, the branch history information of a branch instruction to be requested

to be written is written in said branch prediction unit several clock cycles (several states) after a write request is issued.

32. The method according to claim 26, further comprising:

temporary instruction buffer step temporarily storing an instruction string, etc., outputted by said memory,

wherein if there is no instruction string to be stored in the temporary instruction buffer step and there is no instruction fetch request, the branch history information of a branch instruction to be requested to be written is not promptly written in said branch prediction unit, waits for a next instruction fetch request and is written several clock cycles (several states) after the instruction fetch request is executed.

33. The method according to claim 26, wherein when the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written after its instruction decoding unit or said temporary instruction buffer receives a

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fetch instruction string corresponding to a re-instruction fetch requested by the branch instruction.

34. The method according to claim 26, further comprising:

write reservation station step temporarily storing the branch history information to be written.

35. The method according to claim 34, wherein only the branch history information concerning a branch instruction which must be written in said branch prediction unit is registered in said write reservation station step.

36. The method according to claim 35, wherein the branch history information is a new entry registration, an entry content change or an entry erasure.

37. The method according to claim 34, wherein if a storage capacity in the write reservation station step is full and further there is a register request on a branch instruction, branch history information of which must be written in the write reservation station step, at least one group of a branch history

information, writing of which is held in the write reservation station step and the branch history information which has been requested to be registered, is written.

38. The method according to claim 34, wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and the write reservation station unit stores a plurality of valid information, writing of which is held, a plurality of writing executions are performed in a timing such that writing in said branch prediction unit is available.

39. The method according to claim 26 or 34, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, etc., which exists before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed and even if the branch instruction cannot be completed, the branch history information of the branch instruction is written in said branch prediction unit or registered in the reservation station step.

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40. The method according to claim 39, wherein a flag indicating that the branch history information is written or registered in said write reservation station step is provided for each corresponding branch instruction being processed.

41. An instruction control method in an apparatus provided with both a branch prediction unit performing a branch prediction of a branch instruction and a return address stack, comprising:

controlling in such a way to write branch history information in said branch prediction unit, but not to operate the return address stack if a branch instruction has not been executed although a request for writing of the branch history information in the branch prediction unit is issued by an instruction corresponding to a sub-routine call or return obtained as an execution result of the branch instruction.

42. The method according to claim 34, wherein branch history information, writing of which is held in said write reservation station step, is written when an execution of an instruction is completed.

43. The method according to claim 34, wherein branch

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history information of a corresponding entry is written in said write reservation station unit when an execution of an instruction is completed.

44. The method according to claim 34, wherein an instruction control unit further comprises the step of managing an execution completion of an instruction, and stores an ID assigned for each instruction which is stored in said execution completion management step, in an entry in said write reservation station step.

45. The method according to claim 34, wherein if it is found that a branch instruction corresponding to a valid entry stored in said write reservation station step due to an occurrence of interruption, etc., is not executed and completed, a corresponding entry stored in said write reservation station step is nullified.

46. The method according to claim 26, wherein branch history information, writing of which in said branch prediction unit is held, is a search target of a branch prediction.

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47. The method according to claim 34, wherein branch history information of a branch instruction which is being executed in said write reservation station step, is a search target of a branch prediction.

48. The method according to claim 47, wherein the branch history information is a search target of a branch prediction when a conditional code for the branch instruction is confirmed if it is confirmed that the branch instruction is not branched, and when a branch destination address is confirmed if it is confirmed that the branch instruction is branched.